ance with an overall PCB thickness. In this case, a desired thickness of 0.062 in is achieved by finding a combination of dielectric heights that match both the mechanical and electrical requirements.

The materials specifications mentioned here are approximations and vary between PCB vendors. Before beginning a PCB layout, always select a reputable vendor and confirm the layer stack-up to be sure that your desired impedance can be achieved with the expected dimensions. A vendor should be capable of quoting a stack-up that provides detailed specifications for the trace width and dielectric heights so that your layout can be executed knowing that the design goals are realistic. After accounting for various manufacturing variances, the vendor should be able to deliver controlled impedance traces to an accuracy of ±10 percent or better.

A signal must often change layers as it travels, because of obstructions caused by other devices and other groups of traces that are competing for their journey across the same area of circuit board. Vias are small metal-plated holes that are fabricated into the PCB to allow a signal to change layers as it is routed across a board. When a signal moves between layers, its return current moves with it if the two signal layers do not share a common return plane. For example, signal layers 3 and 4 share a common return plane in Fig. 18.4, but signal layers 1 and 4 do not. A discontinuity results when the return current is not presented with a low-impedance path to follow the signal's layer change. Discontinuities may result in nonideal transmission line behavior, such as reflections and increased noise radiation and susceptibility. Such discontinuities will be mentioned again later in the context of grounding and electromagnetic interference.

High-frequency signals in the gigahertz range can also be adversely affected as traces change direction. It is necessary for a trace to change direction so that it can route a signal to its load. However, the manner in which a corner is created has an effect on the transmission line's characteristic impedance. Recall that Z_O is a function of the trace's capacitance and inductance. A straight trace has approximately constant cross section throughout its length, resulting in constant Z_O. If a trace turns a 90° corner, its cross section changes as shown in Fig. 18.5. Changing cross section, or width, results in different capacitance and inductance. The ideal situation is for a trace to smoothly curve around corners to maintain constant cross section. Although this is usually done for the most demanding very high-speed circuits, it is uncommon for normal digital signals because of the burden that smooth curves place on conventional PCB design software. Imperfections due to corners are negligible for typical digital signals into the hundreds of megahertz. An alternative to a smooth curve is implementing a 45° compromise to provide less of a disruption as compared to a 90° turn, but not quite the cleanliness of a true curve.

Selecting the characteristic impedance for a PCB design is usually done according to industry conventions, because certain connectors and cables are specifically designed with 50- or 75-Ω impedances. Many coaxial cables, particularly in video applications, are 75 Ω, and it is convenient to minimize impedance discontinuities by matching the PCB to the cable. Most high-speed digital cir-

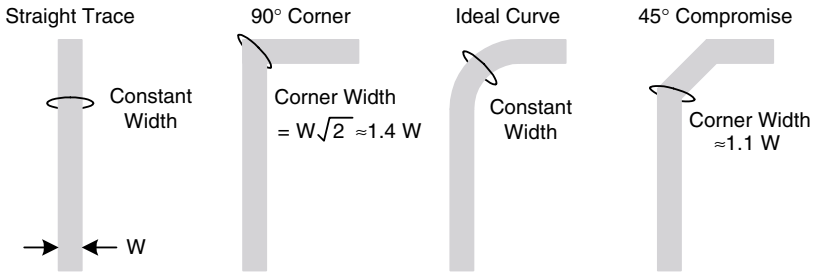

FIGURE 18.5 Effect of corners on trace impedance.

cuits use 50-Ω transmission lines, and some connectors are available with this impedance as well. There are advantages and disadvantages in using higher- or lower-impedance transmission lines. A lower-impedance transmission line requires a thinner dielectric between the signal and return paths. This smaller gap makes the transmission line less susceptible to radiating and coupling noise. It also allows multilayer circuit boards to be made thinner. The disadvantage of lower-impedance transmission lines is that they require higher drive current. Most ICs are capable of driving 50-Ω transmission lines, and high-speed design makes the trade-off of improved noise immunity worth the added power consumption. However, slower circuits may be more suited to 75-Ω transmission lines for power savings.

18.2 TERMINATION

In applying transmission line theory to a digital signal, one should first determine whether the combination of signal transition speed and wire length combine to merit transmission line analysis. Digital signals are characterized not only by their repetitive frequency but also by the frequency components in their edges. A signal with a rapid transition time will have high-frequency components regardless of how long the repetition period. Rules of thumb vary, but a common reference point is to treat a wire as a transmission line if the signal's rise time is less than four times the propagation delay of the wire. The common definition of rise time is the time that the signal takes to transition from 10 to 90 percent of its full amplitude. If the signal transitions slowly with respect to the wire delay, it can be assumed that all points on the wire transition together as the applied signal transitions. When a signal transitions quickly and the wire is long relative to this time, the wire should be treated as a transmission line. It is now common to see signals that transition in 1 ns, meaning that wires with propagation delays greater than 250 ps (about 1.5 in, or 38 mm) require transmission line analysis!

There are several basic termination schemes and numerous variant schemes that have been designed for special digital signaling standards. From our previous discussion of the reflection coefficient, the first obvious termination scheme is to place a resistor equal to Z_O at the end of a transmission line as shown in Fig. 18.6. This is known as *parallel termination*. Note that a transmission line is identified using a graphical representation of a coaxial cable. This does not mean that a transmission line must be implemented as such, but it conveys the idea that the wire length is nonnegligible and cannot be treated as a single node of constant voltage as other wires are. A ground is explicitly connected to the transmission line return path to clearly indicate the circuit's return path. Assuming ideal conditions where Z_O is exactly known, $R = Z_O$, the output impedance of the driver is 0 Ω, and there is no stray capacitance or inductance at either end of the transmission line, parallel termination yields $\Gamma = 0$, and no reflections are present. Of course, these ideal conditions are never achieved, and real terminated transmission lines have some degree of imperfection. The goal is not

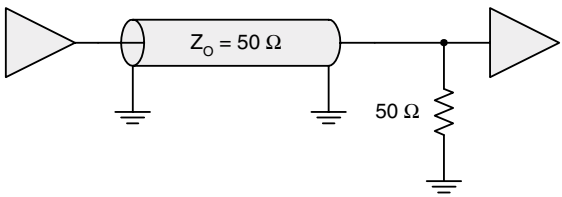

FIGURE 18.6 Parallel termination.